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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/652,834
Filing Date: August 31, 2000
Appellant(s): BERTONE ET AL.

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 21 December 2004.

1. ***Real Party in Interest***

A statement identifying the real party in interest is contained within the brief.

2. ***Related Appeals and Interferences***

A statement indicating Applicant is unaware of any related appeals or interferences is contained within the brief.

3. ***Status of Claims***

The statement of the status of the claims contained within the brief is correct.

4. ***Statement of Amendments After Final***

The Appellant's statement of the status of amendments after final rejection contained within the brief is correct.

5. ***Summary of Invention***

The summary of the invention contained within the brief is correct.

6. ***Issues – Grounds of Rejection to Be Reviewed on Appeal***

The Appellant's statement of the issues within the brief is correct.

7. ***Grouping of Claims***

The rejection of Claims 1-16 stand or fall together because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

8. *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

9. *Prior Art of Record*

Examiner relied upon the following prior art in the rejection of the claims under appeal:

US 6,496,917 B1	Cherabuddi	02-2000
5,895,484	Arimilli	04-1997

10. *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims as follows:

Claims 1, 5, 10, 11 & 14 are rejected under 35 U.S.C. § 103(a).

Claims 2 & 6 are rejected under 35 U.S.C. § 103(a).

Claims 3 & 7 are rejected under 35 U.S.C. § 103(a).

Claims 4, 8, 12, 13, 15 & 16 are rejected under 35 U.S.C. § 103(a).

Claim 9 is rejected under 35 U.S.C. § 103(a).

The above rejections are set forth in a prior Office Action mailed on 13 September 2004. The art rejections from the Office Action are reproduced below:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent US 6,496,917 B1 to Cherabuddi in view of US Patent 5,895,484 to Arimilli.

3. Regarding Claims 1, 5 and 10, Cherabuddi discloses a distributed multiprocessing computer system, comprising: a plurality of processor nodes each coupled to an associated memory module, wherein each memory module may store data that is shared between said processor nodes; a Home processor node that includes a data block and a coherence directory for said data block in an associated memory module; on Owner processor node that includes a copy of said data block in a memory module associated with the Owner processor node, said copy of said data block residing exclusively in said memory module; a Requestor processor node that encounters a read or write miss of said data block and requests said data block from the Home processor node; and wherein said Home processor node receives the request for the data block from the Requestor processor node, forwards the request to the Owner processor node for the data block and performs a speculative write of the next directory state to the coherence directory for the data block without waiting for the Owner processor node to respond to the request (Abstract; Col. 2, lines 66-67; and Col. 3, lines 1-35).

4. Though Cherabuddi discloses a system capable of speculative cache consistency through a snoop information means, Cherabuddi does not specifically teach Applicant's alternative method of a cache directory.

5. Arimilli specifically teaches a method and system for speculatively sourcing cache memory data, (Abstract), that includes a cache directory lookup functionality, (Fig. 2; Col. 4, lines 6-23), and the speculative sourcing of data among cache memories, (Fig. 3; Col. 4, lines 60-67 and Col. 5, lines 1-9). It would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to incorporate a speculatively updateable cache directory into the Cherabuddi system as noted within Arimilli.

6. The motivation to combine lies in the desirability to provide an improved sourcing scheme (method and system) for sharing data among cache memories, (Aramilli – Col. 1, lines 58-67). Moreover, as noted herein, Cherabuddi does teach one of many means by which to maintain speculative cache consistency, therefore the basic functionality is already incorporated by implication. Thus, Examiner rejects Claims 1, 5 and 10 as unpatentable, finding them to be an obvious variation in light of the combined teachings of Cherabuddi in view of Aramilli.

7. Regarding Claims 2 & 6, Cherabuddi and Aramilli are relied upon for those teachings disclosed herein. Cherabuddi discloses a distributed computer system wherein the speculative write of the next directory state occurs only if the next directory state cannot be determined and the Home processor node and Owner processor node are two different processor chips in the computer system, (Col. 3, lines 1-34). Arimilli

specifically teaches a method and system for speculatively sourcing cache memory data, (Abstract), that includes a cache directory lookup functionality, (Fig. 2; Col. 4, lines 6-23), and the speculative sourcing of data among cache memories, (Fig. 3; Col. 4, lines 60-67 and Col. 5, lines 1-9). It would have been obvious to combine Cherabuddi and Aramilli, the motivation for which is disclosed herein above. Thus, Examiner rejects Claims 2 & 6 as unpatentable, finding them to be an obvious variation in light of the combined teachings of Cherabuddi in view of Aramilli.

8. Regarding Claims 3 & 7, Cherabuddi and Aramilli are relied upon for those teachings disclosed herein. Cherabuddi discloses a distributed multiprocessing computer system wherein the memory module containing the coherence directory for the data block is in a low latency state that reduces memory read and write access times while the Home processor node is performing the speculative write of the next directory state to the coherence directory for the data block, (Col. 3, lines 29-35 and Col. 4, lines 25-61). Arimilli specifically teaches a method and system for speculatively sourcing cache memory data, (Abstract), that includes a cache directory lookup functionality, (Fig. 2; Col. 4, lines 6-23), and the speculative sourcing of data among cache memories, (Fig. 3; Col. 4, lines 60-67 and Col. 5, lines 1-9). It would have been obvious to combine Cherabuddi and Aramilli, the motivation for which is disclosed herein above. Thus, Examiner rejects Claims 3 & 7 as unpatentable, finding them to be an obvious variation in light of the combined teachings of Cherabuddi in view of Aramilli.

9. Regarding Claims 4 & 8, Cherabuddi and Aramilli are relied upon for those teachings disclosed herein. Cherabuddi discloses a distributed multiprocessing

computer system wherein the next directory state for the data block is corrected if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block, (Col. 3, lines 1-35 and Col. 4, lines 25-61). Arimilli specifically teaches a method and system for speculatively sourcing cache memory data, (Abstract), that includes a cache directory lookup functionality, (Fig. 2; Col. 4, lines 6-23), and the speculative sourcing of data among cache memories, (Fig. 3; Col. 4, lines 60-67 and Col. 5, lines 1-9). It would have been obvious to combine Cherabuddi and Aramilli, the motivation for which is disclosed herein above. Thus, Examiner rejects Claims 4 & 8 as unpatentable, finding them to be an obvious variation in light of the combined teachings of Cherabuddi in view of Aramilli.

10. Regarding Claim 9, Cherabuddi and Aramilli are relied upon for those teachings disclosed herein. Cherabuddi discloses a distributed multiprocessing computer system wherein the speculative write of the next directory state releases hardware contained in the first processor node, allowing said first processor node to accept requests for data blocks and coherency directories for said data blocks stored in the memory module for the first processor node, (Col. 4, lines 62-67 and Col. 5, lines 1-6). Arimilli specifically teaches a method and system for speculatively sourcing cache memory data, (Abstract), that includes a cache directory lookup functionality, (Fig. 2; Col. 4, lines 6-23), and the speculative sourcing of data among cache memories, (Fig. 3; Col. 4, lines 60-67 and Col. 5, lines 1-9). It would have been obvious to combine Cherabuddi and

Aramilli, the motivation for which is disclosed herein above. Thus, Examiner rejects Claim 9 as unpatentable, finding them to be an obvious variation in light of the combined teachings of Cherabuddi in view of Aramilli.

11. New Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent US 6,496,917 B1 to Cherabuddi in view of US Patent 5,895,484 to Arimilli.

12. Regarding new Claims 11 & 14, all limitations are addressed relative to Claims 1, 5 and 10 above. Thus, Claims 11 & 14 are also rejected under the combined teachings of Cherabuddi in view of Aramilli.

13. Regarding new Claims 12, 13, 15 and 16, all limitations are addressed relative to Claims 4 & 8 above. Thus, Claims 12, 13, 15 and 16 are also rejected under the combined teachings of Cherabuddi in view of Aramilli.

11. *Response to Arguments*

11.1 A. Overview of Cherabuddi

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "cache directories, reading or writing from cache directories, or even speculatively reading/writing cache directories." (Appeal Brief: p.11, lines 1-2).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses "cache directories, reading or writing from cache directories, or even speculatively reading/writing cache directories", as quoted from paragraph 16 of the Final Office Action:

> Examiner finds that Cherabuddi discloses a system capable of speculative cache consistency through a snoop information means; however, Cherabuddi does not specifically teach Applicant's alternative method of a cache directory, which alternative method would have been obvious as noted above. Moreover, Examiner finds that it is the combined teachings of Cherabuddi in view of Arimilli that render Applicant's invention unpatentable. Clearly Cherabuddi discloses a speculation means, which means could have obviously been combined with the Arimilli system as part of either "cache housekeeping" or "updating directory of L2 cache", (Fig. 3), per Claims 5, 10 & 11. Additionally, Examiner notes that the Cherabuddi memory means would obviously include a directory table for address location purposes. Further, Arimilli discloses directory tables, and the combination of Cherabuddi and Arimilli would have been obvious as noted herein.

Moreover, Examiner notes that Cherabuddi discloses a multiprocessor computer system capable of reducing primary memory latencies by routing speculative address requests directly from the external cache controller to the memory interface unit via the CPU in response to external cache misses. Cherabuddi further teaches a "snoop" means by which CPUs monitor the system bus for information pertaining to one another, wherein maximum performance is achieved when data corresponding to speculative address requests is retrieved from primary memory as or before bus ordering information and snoop information becomes available, (Cherabuddi - Col. 4, lines 22-67 & Col. 5, lines 1-45). Thus, Examiner notes that Cherabuddi clearly discloses a method for maintaining data coherency through speculatively writing data, which data remains speculative until validated. Further, Examiner notes that within this section of the brief, Appellant limits their focus of Cherabuddi deficiencies to that of lacking a speculative read/write to cache directories for purposes of maintaining data coherency.

11.1 B. Overview of Arimilli

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively reading and writing data from memory" (Appeal Brief: p.11, lines 20-24).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory.

Moreover, Examiner notes that Arimilli specifically teaches an improved method for speculatively sourcing data among cache memories within a data-processing system with multiple processing units, each of the processing units including at least one cache memory, wherein, in response to a request for data by a first processing unit within the data-processing system, an intervention response is issued from a second processing unit within the data-processing system that contains the requested data. The requested data is then read from the cache memory within the second processing unit before a combined response from all the processing units returns to the second processing unit, (Arimilli - Col. 2, lines 4-19). Thus, Examiner notes that Arimilli clearly discloses a method for speculatively accessing cache memory, (via intervention response), through both read or "read with the intent to modify", (RWITM), requests, which RWITM requests, like any modification, clearly require a writing. Further, Examiner notes that within this section of the brief, Appellant limits their focus of Arimilli deficiencies to that of lacking a speculative write to cache directories for purposes of maintaining data coherency.

Appellant argues that the directory update in Arimilli is not done speculatively, and Examiner respectfully disagrees. Specifically Examiner notes that Applicant's use of the term "speculative" throughout the specification is within the context of maintaining data coherency when a data state is not able to be determined. As such, Applicant teaches a speculative write of the next directory state, which write requires validation via directory state affirmation, (Appeal Brief, pp. 6-7). Examiner reiterates that Cherabuddi teaches this exact concept, as noted herein above with reference to "external cache misses". Additionally, Examiner notes that Arimilli discloses an "intervention response" followed by "cache housekeeping", both which occur prior to the retry, (Arimilli - Fig. 3), and as such, clearly read upon Appellant's use and application of the term "speculative", particularly in light of the "flushing and/or invalidating of data copy" upon determination of data modification, (Arimilli – Col. 5, lines 10-17). Moreover, the flushing or invalidaing of data copy within a cache inherently requires notation of the same within the cache directory for purposes of maintaining data coherency. Thus, in light of Appellant's use of the term "speculative", Examiner maintains the belief that the combined teachings of Cherabuddi in view of Arimilli clearly disclose a "speculative write to cache directories", as noted herein above.

11.1 C. Claims 1, 3, 5, 7 & 10

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively writing a next directory state" (Appeal Brief: p.12, lines 4-5).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation, as noted within MPEP § 2145 (IV), which reads as follows:

> One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., Inc., 800 F.2d 1091, 231 USPQ 375 Fed. Cir. 1986).

Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 B (supra), which discusses "speculative writing to cache directories".

11.1 D. Claim 11

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively writing a next directory state before receiving a coherence response from the owner" (Appeal Brief: p.12, lines 16-18).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 C (supra), which discusses "speculative writing, (intervention response) to cache directories prior to receipt of combined response", (Col. 4, lines 6-35). Examiner notes

that the combined response inherently includes a response from all processing units, other than the requesting unit, which group obviously includes the owner-processing unit.

11.1 E. Claim 14

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively writing a next directory state before receiving a coherence response from the owner" (Appeal Brief: p.12, lines 26-28).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 D (supra), which discusses "speculative writing, (intervention response) to cache directories prior to receipt of combined response", (Arimilli - Col. 4, lines 6-35). Examiner notes that the combined response inherently includes a response from all processing units, other than the requesting unit, which group obviously includes the owner-processing unit.

11.1 F. Claims 2 & 6

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively writing a next directory state only if the next directory state can not be determined and the Home processor node and Owner processor node are two different processor chips in the computer system" (Appeal Brief: p.14, lines 5-8).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 E (supra), which discusses speculative writing per a "cache miss", (Cherabuddi, Col. 3, lines 5-23). Additionally, Examiner notes that the combined teachings of Cherabuddi and Arimilli obviously include all circumstances for processor combination locations, including, but not limited to the home processor and owner processor existing on separate chips, (Arimilli – Col. 3, lines 46-59). That noted, Examiner further finds that it would be obviously unnecessary for a speculative write wherein the Home processor node and Owner processor node are on the same processor chip as the same would not be "speculative" in light of the Home processor node having possession of the data in its most current and accurate state, thereby not requiring validation of the same.

11.1 G. Claims 4 & 8

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' "
(Appeal Brief: p. 16, lines 14-19).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 F (supra), which discusses correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block', (Cherabuddi - Col. 4, lines 35-67 & Col. 5, lines 1-22). Examiner particularly points out that the validation process enumerated within Cherabuddi clearly acts as a correction mechanism for purposes of data coherency.

11.1 H. Claim 9

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "a speculative directory state write causing the release of hardware" (Appeal Brief: p.17, lines 9-10).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's argument 11.1 A - 11.1 G (supra), which discusses "speculative writing, (intervention response) to cache

directories", (Arimilli - Col. 4, lines 6-35). Examiner notes that the fulfillment of a request with a speculative write releases the processing unit (completing said request) from a continued wait, (Arimilli – Col. 1, lines 38-46), thereby allowing said processor to attend to other requests. Examiner further notes that this is the functionality Appellant relies upon within Claim 9.

11.1 I. Claim 12

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "speculatively writing the directory state before receiving a coherence response" and "correcting, (rewriting) the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' " (Appeal Brief: p. 17, lines 17-20).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's arguments 11.1 A - 11.1 H (supra), which discuss "speculatively writing the directory state before receiving a coherence response" and "correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence

directory for the data block' ". Examiner notes that the validation process inherently includes a confirmation of speculatively written data.

11.1 J. Claim 13

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "correcting, (rewriting) the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' " (Appeal Brief: p. 17, lines 30-31).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's arguments 11.1 A - 11.1 I (supra), which discuss "correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' ". Examiner notes that the validation process inherently includes a confirmation of speculatively written data.

11.1 K. Claim 15

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "correcting, (rewriting/confirming) the next directory state under the stated condition which is 'if the

response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' " (Appeal Brief: p. 18, lines 10-17).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's arguments 11.1 A - 11.1 J (supra), which discuss "correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' ". Examiner notes that the validation process inherently includes a confirmation of speculatively written data.

11.1 L. Claim 16

Cherabuddi '917 in combination with Arimilli '484 in fact discloses "correcting, (rewriting/confirming) the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' " (Appeal Brief: p. 18, lines 27-30).

Examiner points out that it is not enough to assert that Cherabuddi '917 does not disclose a claimed limitation. Rather, the Applicant must show that the combination of

references does not disclose the claimed limitation. Cherabuddi '917 in combination with Arimilli '484 in fact discloses speculatively reading and writing data from memory. Additionally, Examiner reiterates counter-argument to Appellant's arguments 11.1 A - 11.1 K (supra), which discuss "correcting the next directory state under the stated condition which is 'if the response by the Owner processor node to the Home processor node request for the data block indicates a different next directory state from the next directory state speculatively written by the Home processor node to the coherence directory for the data block' ". Examiner notes that the validation process inherently includes a confirmation of speculatively written data.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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